Next Generation Digital LLRF Platform at PSI

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Roger Kalt – Paul Scherrer Institut

Abstract

The High-Intensity Proton Accelerator (50, 150 MHz CW) and the Swiss Light Source (500 MHz, CW and long-pulsed) analog LLRF system require an upgrade to a digital system. As a key requirement, the selected digital processing platform for LLRF systems must fit into the lab's control system environment.

Three different generic digital processing platforms were evaluated with respect to the LLRF requirements. They include CPCI-S.0, MTCA.4 and a full-custom in-house crate design. The pro's and con's of the different approach are compared.

Pre-Selection

Up to now the PSI bus standard used in the control systems in the machines HIPA, SLS, Proscan and SwissFEL is VME. Analysis of the current installations showed, that the majority of the VME 21- and 7-slot crates are used less than 50%. The majority of the usage is still slave I/O cards for slow and standard type I/O like 0-10V, 4-20mA or 0V/5V/24V.

Nowadays such type of standard I/O with a slow sampling rate up to several hundred Hz is possible to implement with industrial type network attached I/O devices like e.g. from Wago or Beckhoff. On the other hand the VME slave boards hardware for such application type are discontinued and no longer available on the market.

Bus Platform Evaluation for Control System

For the remaining applications and systems which need to be covered by the control system toolbox, a bus platform study group was created. Based on definition of criteria and weights agreed on by the PSI management, CompactPCI Serial is presently being evaluated as possible future bus- and crate-standard for PSI. For this comparable new standard, different manufacturers for COTS hardware like CPU system controllers, XMC carriers, AIO, and DIO cards are already available, and significant future growth is expected. The partly PSI specific selection criteria for the crate standard evaluation include future usage & perspectives, complexity, features and technology.

Proposal for detailed evaluation new platform:

1. **CompactPCI Serial**
2. VPX
3. VME64x
4. MTCA.4
5. MTCA.0/AMC

Data Processing Platform for all Applications

The use of a popular CPU architecture is an essential point. Compared to the currently used PowerPC in the PSI VME bus system controllers, other architectures like ARM or Intel receive better support from the Open Source community. This is important for the generic part like OS (e.g. Linux kernel) or hardware device drivers (e.g. for network PHY chips).

Since the control system already nowadays runs with many EPICS softIOC's on virtual servers, the Intel X86_64 CPUs allows to minimize additional internal effort for creation and maintenance of dedicated board-support-packages.

Selection:	Architecture
CPU-only systems:	Intel x86_64
FPGA-only systems:	Xilinx (all families)
FPGA+CPU systems	Xilinx Zynq US+

For deeply embedded applications which are not located inside the CPCI-S crate but need CPU based data processing, the selection was made to Xilinx Zynq UltraScale+ FPGAs with embedded hardcore ARM cores. Dependent on the required number and type of I/Os, COTS SoM (System-on-Module) can be used.

Next Platform Evaluation Candidates for LLRF

Figure 1: MTCA.4 Crate, Schoff/nvent

Figure 2: CPCI-S Crate, ADLinkTech

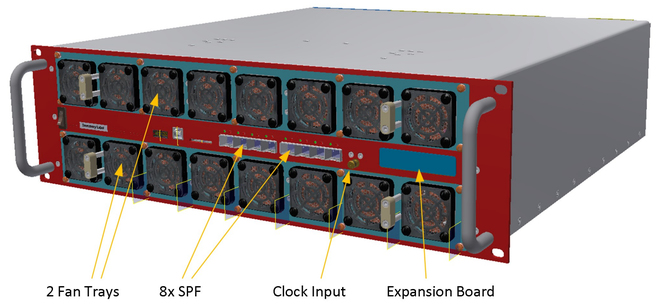
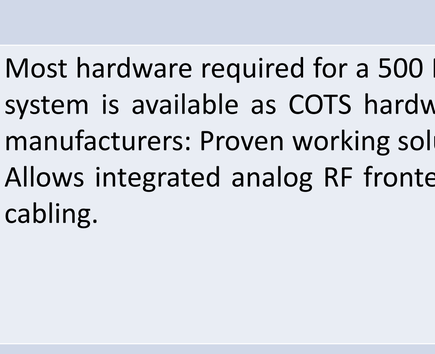
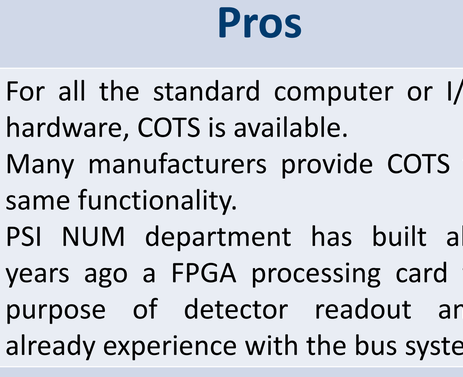
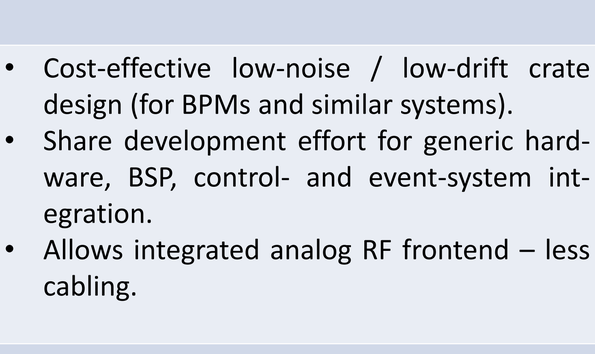


Figure 3: DBPM3 Crate, PSI

MicroTCA.4	CompactPCI Serial	PSI DBPM3
Short Description		
MicroTCA is a standard for modular embedded computer systems. The standard is governed by the PICMG group. The extension MicroTCA for Physics (MTCA.4) defines a direct rear I/O without passing the backplane for the purpose of integration of the analog frontend into the same crate on rear boards. The use of an additional specific LLRF / RF backplane e.g. for ADC or LO clocks distribution is an optional feature.	CompactPCI Serial is a standard for modular industrial computer systems. The standard is governed by the PICMG group. The standard backplane specifies only a part of the connectors and leaves freedom to define custom rear I/O.	For more than 200 new BPM in the SLS2.0 and SwissFEL, PSI designed a custom crate that is more cost-effective and performant than standard crate solutions. Up to six RF front-end modules with integrated ADC/DACs can be hot-plugged from the rear side, with coplanar 25Gbps connectors to a single digital-backend board with a Xilinx Zynq UltraSCale+ MPSoC/ FPGA and flexible clocking. Up to 6 RFFEs with 2 JESD204B ADC (Rx) and 2 DAC (Tx) lanes each can be directly interfaced to the back-end.
Availability Status		
LLRF specific COTS hardware is available from some few manufacturers. Small sized MTCA.4 crates are rather new (2019).	Standard computer- or I/O type COTS hardware for 3U systems is available from many manu-facturers.	Prototype of daughter board with ADC and additional BPM RF frontend available now. Prototype of crate and mainboard available in Q4-2019.
Pros		
• Most hardware required for a 500 MHz LLRF system is available as COTS hardware from manufacturers: Proven working solution. • Allows integrated analog RF frontend – less cabling.	• For all the standard computer or I/O type hardware, COTS is available. • Many manufacturers provide COTS for the same functionality. • PSI NUM department has built about 8 years ago a FPGA processing card for the purpose of detector readout and has already experience with the bus system.	• Cost-effective low-noise / low-drift crate design (for BPMs and similar systems). • Share development effort for generic hard-ware, BSP, control- and event-system int-egration. • Allows integrated analog RF frontend – less cabling.
Cons		
• It seems that the BSP for the FPGA digitizer boards is one of the weak points: There are alternative commercial BSP providers or labs implemented their own BSP for the same digitizer board. • Only a few providers of COTS hardware with the same functionality. • Own hardware development would need to build up internal knowledge to avoid pitfalls. • LO / CLK generation own development	• Currently there is no suitable digitizer board available as COTS hardware on the market: Risk of high cost, late delivery. • We should not try to imitate MTCA.4 with an integrated RF backplane or an integrated analog RF frontend: The effort too high • This then also results in keeping the scheme of separated pizza-boxes for the RF front-ends and cabling in between.	• Up to 12 Rx and 12 Tx lanes for JESD204B ADCs and DACs per one crate. Two crates required for a 24-channel LLRF. • The use of ADCs/DACs with parallel IOs would require an additional FPGA on the RF frontend acting as serialize/deserializer. • PSI-specific crate standard, not COTS boards available (yet).
Architecture of 500 MHz LLRF Implementation		
		
Proposed Selection		
After the pre-selection for CPCI-S, it is already known that MTCA.4 is not considered for LLRF. The strategy is, to minimize the different type of systems that require long-term support for BSP, OS, drivers, control system integration.	Remaining Candidate.	Remaining Candidate.

Conclusion / Outlook

Out of the two remaining candidates for the new LLRF systems a selection is planned for Q4-2019. Criteria for this selection are the risk (not meeting functionality or time plan requirements), the priority of other PSI-internal non-LLRF projects and the overall cost. Then the goal for 2020 is to implement a prototype LLRF system for lab characterization and installation at the SLS 500 MHz cavity test stand in 2020/21.

Revision 2, Roger Kalt roger.kalt@psi.ch , 24.09.2019, presented at LLRF Workshop 2019 (LLRF2019, arXiv:1909.06754)